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The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

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Respectfully submitted,

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Dated: September 3, 2004

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Docket No.: 00-387 / 1496.00089

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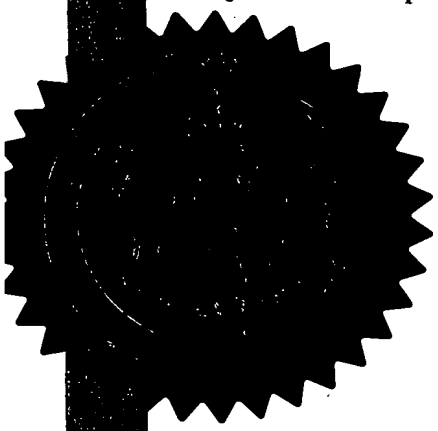

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01NOV00 E580147-1 D01072
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3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

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   Patents ADP number *(if you know it)* — 08869001

   If the applicant is a corporate body, give the country/state of its incorporation — United Kingdom

4. Title of the invention — A method and apparatus for estimation of error in data recovery schemes

5. Name of your agent *(if you have one)* — Hepworth Lawrence Bryer & Bizley

   "Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)* — Merlin House, Falconry Court, Baker's Lane, Epping, Essex CM16 5DQ

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A METHOD AND APPARATUS FOR ESTIMATION OF ERROR IN DATA RECOVERY SCHEMES

FIELD OF THE INVENTION

This invention relates to a method and apparatus for estimation of error in data recovery schemes.

BACKGROUND OF THE INVENTION

In digital data recovery schemes, it is desirable to be able to provide an on-chip method for estimating the quality of the recovered data which is independent of data patterns. This information can then provide a figure of merit for enabling key system parameters to be optimised. The most meaningful measure of channel data quality is the average bit-error-rate (BER) and in some prior art schemes this has been achieved by measuring the frequency of amplitude deviation from a specified reference level.

For example, in US Patent No. 4,234,954, there is disclosed an on-line circuit that estimates the bit error rate (BER) of a binary data signal stream in the presence of noise uncorrelated with the signal. For a binary data signal having two states, e.g., plus V and minus V biased around a specified reference level (REF), the circuit counts the number of instances in which the received signal deviates more than 2V from the reference level. This accumulated count gives an accurate estimate of the BER over several orders of magnitude variation of the BER.

US Patent No. 3,721,959 discloses a method and means of error rate detection including developing an eye pattern analog signal of transmitted digital data, defining a region within said eye pattern as an unacceptable area through which said eye pattern may not transgress, and counting as an erroneous signal each transgression of said analog signal into said region.

The drawback of such schemes is that in the error rate estimation it does not take account of errors induced by clock jitter. A more meaningful method for estimating the channel BER can be obtained by measuring the statistics of the phase errors, i.e. the time between the clock edge and the data edge. Such a method takes into account errors induced by both noise on the input data signal and also clock jitter. As shown in FIG. 1, in an ideal

system the clock signal 1 and the data signal 2 should have edges 3, 4 which are co-incident, but in practice, due, for example, to channel imperfections, the position of the clock edge 5 relative to the data edge 6 will vary (see FIG. 2). Furthermore, the average error may not have a mean of zero. A data error will occur if the time, ΔT (or phase error), between the clock edge 5 and the data edges 6 is > ½ or <-½ , where ΔT has been normalised to the clock period T i.e. if the data falls in the wrong clock window. Thus, knowledge of the phase error statistics enables an estimate of the average channel performance to be predicted. In general, though, the phase noise probability density function (pdf) is not a simple function, typically it will be Gaussian. Therefore, to evaluate the probability of error in a system requires a complex integral to be evaluated.

BRIEF SUMMARY OF THE INVENTION

The present invention therefore seeks to provide a method and apparatus for estimation of error in data recovery schemes, which overcomes, or at least reduces the above-mentioned problems of the prior art.

Accordingly, in a first aspect, the invention provides a method of estimating an error in a data recovery system, the method comprising the steps of receiving data pulses at a data rate, receiving a plurality of clock signals, the clock signals having the same rate as the data rate but being substantially equally phase offset from one another, clocking the data pulses with each of the clock signals to determine at which phase offset each data pulse is received, counting the number of data pulses received at different phase offsets to provide a value representing a statistical ratio of the counts at different clock phase offsets, and utilizing the value representing the statistical ratio to determine an error for the received data pulses.

In a preferred embodiment, the step of clocking the data pulse comprises applying the data pulses to each of a plurality of registers, each clocked by a different one of the plurality of clock signals, and determining which of the plurality of registers first clocks each data pulse.

Preferably, the step of counting the number of data pulses received at different phase offsets comprises incrementing one of a plurality of counters each time a register associated with that counter is determined to have first

clocked a particular data pulse, and determining the count of at least one counter when at least one other counter reaches a predetermined value.

The step of utilizing the value representing the statistical ratio to determine an error preferably comprises checking a look-up table for an error rate corresponding to the value.

In one preferred embodiment, there are four clock signals which are in a quadrature phase relation. The step of counting the number of data pulses received at different phase offsets preferably comprises incrementing a first counter when either one of two registers clocked by clock signals having phase offsets of 0° and 90° first clocks a particular data pulse or incrementing a second counter when either one of two registers clocked by clock signals having phase offsets of 180° and 270° first clocks a particular data pulse, determining when one of the two counters reaches a predetermined value, and determining the count of the other of the two counters; and wherein the count of the other counter is then used to determine an error rate from a look-up table.

Preferably, the step of counting the number of data pulses received at different phase offsets comprises incrementing a first counter when either one of two registers clocked by clock signals having phase offsets of 0° and 270° first clocks a particular data pulse or incrementing a second counter when either one of two registers clocked by clock signals having phase offsets of 90° and 180° first clocks a particular data pulse, determining when one of the two counters reaches a predetermined value, and determining the count of the other of the two counters; and wherein the count of the other counter is then compared to the predetermined value and used to determine whether a skew error is positive or negative.

According to a second aspect, the invention provides an apparatus for estimating an error in a data recovery system, the apparatus comprising a data terminal for receiving data pulses at a data rate, a plurality of clock input terminals for receiving a plurality of clock signals, the clock signals having the same rate as the data rate but being substantially equally phase offset from one another, data clocking device having a data input coupled to the data terminal, a plurality of clock inputs coupled to the plurality of clock input

terminals and a plurality of outputs, each providing a count signal when a data pulse is clocked by a clock signal at an associated clock input, a plurality of counters, each having a count input coupled to at least one of the plurality of outputs of the data clocking means for counting the number of data pulses received at different phase offsets to provide a value representing a statistical ratio of the counts at different clock phase offsets, and a device having an input coupled to the output of at least one of the plurality of counters and an output to provide an error for the received data pulses based on the counts at different clock phase offsets.

In a preferred embodiment, the data clocking means comprises a plurality of registers, each register having a first input coupled to the data input, a second input and an output, each of the second inputs of the plurality of registers being coupled to a different one of the plurality of clock inputs, and a discriminating device having a plurality of inputs coupled to the outputs of the plurality of registers and a second plurality of outputs, wherein only one of the outputs provides a count signal for each data pulse received depending on which register was the first to clock the particular data pulse.

Preferably, at least one counter has a maximum value associated therewith and provides an indication at an output thereof when that maximum value has been reached, and at least one other counter provides at an output thereof an indication of the value it has reached when the at least one counter has reached the maximum value.

In one preferred embodiment, there are four clock signals which are in a quadrature phase relation. Preferably, there are four registers, each receiving one of the four clock signals at the second input thereof.

The discriminating device preferably comprises a four input NOR gate, the four inputs being coupled to the four outputs of the four registers, and an output, four multiplexers, each having a first input coupled to a respective output of a respective one of the four registers, a second input coupled to an output of the multiplexer, and a control input coupled to the output of the NOR gate, four second registers, each of the second registers having a first input coupled to a respective output of a respective multiplexer, a clock input coupled to receive a system clock signal, and an output, and a first OR gate having first and second inputs coupled to the outputs of two of the second

registers and an output, and a second OR gate having first and second inputs coupled to the outputs of the other two of the second registers and an output.

The first OR gate preferably has its first and second inputs coupled to the outputs of the two second registers corresponding to the two registers clocked by clock signals having phase offsets of 0° and 90° and the second OR gate has its first and second inputs coupled to the outputs of the two second registers corresponding to the two registers clocked by clock signals having phase offsets of 180° and 270°.

Preferably, a first counter is incremented when either one of two registers clocked by clock signals having phase offsets of 0° and 90° first clocks a particular data pulse and a second counter is incremented when either one of two registers clocked by clock signals having phase offsets of 180° and 270° first clocks a particular data pulse. The device preferably includes a look-up table which provides an error rate for the received data pulses based on the ratio of the values of the two counters.

Preferably, the first OR gate has its first and second inputs coupled to the outputs of the two second registers corresponding to the two registers clocked by clock signals having phase offsets of 0° and 270° and the second OR gate has its first and second inputs coupled to the outputs of the two second registers corresponding to the two registers clocked by clock signals having phase offsets of 90° and 180°.

In one embodiment, a first counter is incremented when either one of two registers clocked by clock signals having phase offsets of 0° and 270° first clocks a particular data pulse and a second counter is incremented when either one of two registers clocked by clock signals having phase offsets of 90° and 180° first clocks a particular data pulse.

Preferably, the device includes a comparator to determine which of the two counters has a higher value so as to provide an indication of whether a skew error is positive or negative.

BRIEF DESCRIPTION OF THE DRAWINGS

Two embodiments of the invention will now be more fully described, by way of example, with reference to the drawings, of which:

FIG. 1 shows a schematic diagram of clock and data signals in an ideal system;

FIG. 2 shows a schematic diagram of clock and data signals in most real systems;

FIG. 3 shows a graph of a probability density function for Gaussian distributed phase error having a standard deviation of 0.2;

FIG. 4 shows a coarse histogram with spacing of T/4 for the distribution of FIG. 3;

FIG. 5 shows a schematic block diagram of a first embodiment of an apparatus for estimating an error in a data recovery system according to the present invention;

FIG. 6 shows a schematic block diagram of the phase error determination element of FIG. 5 in more detail;

FIG. 7 shows a timing diagram for the phase error determination element of FIG. 6; and

FIG. 8 shows a schematic block diagram of a skew error determination element used in a second embodiment of an apparatus for estimating an error in a data recovery system according to the present invention, similar to that of the phase error determination element of FIG. 5.

DETAILED DESCRIPTION OF THE DRAWINGS

Thus, as shown in FIG. 1, and as described above, in an ideal system the clock signal 1 and the data signal 2 should have edges 3, 4 which are co-incident, but in practice, due, for example, to channel imperfections, the position of the clock edge 5 relative to the data edge 6 will vary (see FIG. 2). A data error will occur if the time, ΔT (or phase error), between the clock edge 5 and the data edges 6 is > ½ or <-½ , where ΔT has been normalised to the clock period T i.e. if the data falls in the wrong clock window. Thus, knowledge of the phase error statistics enables an estimate of the average channel performance to be predicted. In general, though, the phase noise probability density function (pdf) is not a simple function, and typically it will be Gaussian, as shown in FIG. 3.

For this case, if X is a random variable which represents the phase errors in a system and if it is assumed that X is Gaussian distributed with a mean $\mu = 0$ and variance σ^2, then the pdf is given by:

$$p(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{x^2}{2\sigma^2}}$$

Therefore the probability of a phase error > α is:

$$\text{Prob}\,(X > \alpha) = \frac{1}{\sigma\sqrt{2\pi}} \int_{\alpha}^{\infty} e^{-\frac{x^2}{2\sigma^2}}\, dx \qquad (1)$$

It should be noted that Prob ($X > \alpha$) = Prob ($X < -\alpha$)

Given that an error is made if $|\Delta T| > ½$ from equation (1), the following equation for the probability of error, P_{err} can be obtained:

$$P_{err} = \frac{1}{K}\left(\frac{1}{\sigma\sqrt{2\pi}} \int_{\frac{1}{2}}^{\infty} e^{-\frac{x^2}{2\sigma^2}}\, dx + \frac{1}{\sigma\sqrt{2\pi}} \int_{-\infty}^{-\frac{1}{2}} e^{-\frac{x^2}{2\sigma^2}}\, dx \right) \qquad (2)$$

which may be written as:

$$P_{err} = \frac{2}{K\sigma\sqrt{2\pi}} \int_{\frac{1}{2}}^{\infty} e^{-\frac{x^2}{2\sigma^2}} dx \qquad (3)$$

where K is a constant representing the average rate of phase error updates normalised to the clock period.

Similarly, the following equation for the probability of $|\Delta T| > ¼$ can be obtained:

$$\text{Prob}\left(|\Delta T| > \frac{T}{4} \right) = \frac{2}{\sigma\sqrt{2\pi}} \int_{\frac{1}{4}}^{\infty} e^{-\frac{x^2}{2\sigma^2}} dx \qquad (4)$$

and

$$\text{Prob}\left(|\Delta T| < \frac{T}{4} \right) = 1 - \frac{2}{\sigma\sqrt{2\pi}} \int_{\frac{1}{4}}^{\infty} e^{-\frac{x^2}{2\sigma^2}} dx \qquad (5)$$

For various values of σ, the corresponding values of equations (3) and (5) can be tabulated, as shown in Table 1, which shows these values for $K = 5$.

σ	equation(3)	equation(5)
0.1	$1x10^{-7}$	0.9875
0.11	$1x10^{-6}$	0.977
0.125	$1x10^{-5}$	0.9545
0.145	$1x10^{-4}$	0.9150
0.18	$1x10^{-3}$	0.8350
0.2575	$1x10^{-2}$	0.6666

Table 1

Thus, if an estimate for the value of equation (5) can be deduced, then, with the aid of Table 1, the corresponding value for equation (3) and hence an estimate of the error rate can be found.

To find an estimate for the value of equation (5), the data edge pulse is clocked with four clocks running at the data rate but in quadrature phase denoted as clk0, clk90, clk180 and clk270. The four clock phases can be used to create a coarse histogram of the phase error distribution where the resolution is *T*/4. FIG. 3 shows the pdf for a Gaussian distributed phase error with $\sigma = 0.2$ and FIG. 4 shows a coarse histogram with spacing *T*/4 for the same distribution. In FIG. 3 the terms A0, A1, A2, A3, A4 and A5 represent the areas under the curve in the x-axis regions $\Delta T < -\frac{1}{2}$, $-\frac{1}{2} \leq \Delta T < -\frac{1}{4}$, $-\frac{1}{4} \leq \Delta T < 0$, $0 \leq \Delta T < \frac{1}{4}$, $\frac{1}{4} \leq \Delta T < \frac{1}{2}$ and $\Delta T > \frac{1}{2}$ respectively. In FIG. 4 the terms H0, H1, H2, H3, H4 and H5 represent the heights of the histogram columns which are equivalent to the areas A0, A1, A2, A3, A4 and A5 in FIG. 3 i.e. the probability of a phase error falling in these regions. The Prob($|\Delta T| < T/4$) can be defined as :

$$\text{Prob}\left(|\Delta T| < \frac{T}{4}\right) = A2 + A3 \qquad (6)$$

An estimate for the term A2 +A3 can be deduced using the four quadrature phase clocks, whereby an estimate for equation (5) can be found and hence an estimate for equation (3). One embodiment of an apparatus which can be used to calculate A2+A3 will now be described.

FIG. 4 shows an outline block diagram of an apparatus 10 having a phase error window block 11, a pair of counters 12 and 13, a comparator 14, a register 15, and a memory 16 having a look-up table stored therein. The phase error window block 11 receives four clock inputs, which are in quadrature with each other, labelled clk0, clk90, clk180 and clk270 and a data edge pulse, and determines which phase window the phase error falls into and provides signals which update the counters 12 and 13. The first (N-bit) counter 12 records the number of phase errors which fall into the windows - ¼ ≤ ΔT < 0 and 0 ≤ ΔT < ¼ (e.g. n2+n3) and the second (M-bit) counter 13 records the number of phase errors falling into the windows - ½ ≤ ΔT < - ¼ and ¼ ≤ ΔT < ½ (e.g. n1+n4). The comparator 13 is used to determine when the first counter 12 reaches its limit of $2^N - 1$. When this occurs, the value in the second counter 13 is latched into the register 15 and both counters 12 and 13 are reset for the process to be repeated. The latched value in register 15 is then used to estimate A2+A3 as:

$$A2 + A3 \approx \frac{n2 + n3}{n1 + n2 + n3 + n4} = \frac{2^N - 1}{2^N - 1 + n1 + n4} \qquad (7)$$

The approximation can be used because although phase errors of the type $|\Delta T| > ½$, i.e the terms A0 and A5 in the Gaussian curve of FIG. 3, are not guaranteed to be counted correctly, these occurrences will be relatively rare and can be ignored as they will have a negligible effect on accuracy. Equation (7) can thus be used with the aid of a look-up table to deduce the error rate. Clearly, if *N* is fixed, then the look-up table can simply map the value of n1+n4 to a precalculated error rate stored in the memory 16. The size of the first and second counters 12 and 13 is dependent on the error rate range over which the measurements are to operate and the required accuracy. To cater for error rate ranges from 10^{-2} to 10^{-7}, a value of N of 10 and a value of M of 8 is sufficient to provide good accuracy and would provide a new error rate estimation update approximately every 1100 phase error comparisons (the actual frequency would be dependent on the channel noise).

Further details of the phase error window block 11 are shown in FIG. 6, which shows the four quadrature clocks clk0, clk90, clk180 and clk270 and

the data pulse signals being provided at inputs 17, 18, 19, 20 and 21, respectively. The data pulse is applied to a first set of four registers 22, 23, 24 and 25, each register being clocked with one of the four clock phases clk0, clk90, clk180 and clk270. For each data pulse, the output from the first set of four registers 22, 23, 24 and 25 will typically produce four pulses q0, q90, q180 and q270 spaced T/4 apart. The outputs of the four registers 22, 23, 24 and 25 are applied to a 4-input NOR gate 26 and to a set of four multiplexers 27, 28, 29 and 30, respectively. The multiplexers' select lines are controlled by the output of the NOR gate 26 and their outputs are fedback to their respective second inputs. Thus, the function of the multiplexers 27, 28, 29 and 30 and the 4-input NOR gate 26 is to provide at the outputs of the multiplexers a "1" at the output of the multiplexer coupled to the register which first clocked the data pulse input, and a "0" at all the other outputs.

The outputs of the respective multiplexers 27, 28, 29 and 30 are applied to respective inputs of four registers 31, 32, 33 and 34 forming a second set of registers. The second set of registers is clocked by the main system clock i.e. clk0. The outputs of the second set of registers are applied to two OR gates 35 and 36. By coupling the outputs of the appropriate registers 31, 32, 33 and 34 into the appropriate OR gates, the data pulses within appropriate phase windows are combined so that appropriate counters 12 or 13 are updated. Thus, in this case, the outputs of registers 31 and 32, corresponding to the phase windows clocked by clocks clk0 and clk90, are coupled to OR gate 35 to provide an "update inner" signal to counter 12 and the outputs of registers 33 and 34, corresponding to the phase windows clocked by clocks clk180 and clk270, are coupled to OR gate 36 to provide an "update outer" signal to counter 13. When no data edge pulses are present then no updates are made to the counters.

FIG. 7 shows some of the signals for the circuit of FIG. 6 for an example data pulse. The four quadrature clocks are shown as clk270, clk180, clk90 and clk0, and an input data pulse being shown as a data signal. The first of the four clock phases to clock the data pulse, in this example, is clk180. This results in the output signal r180 from register 33 going high on the next positive edge of clk0, while the output signals r270, r90 and r0 at the outputs of registers 34, 32 sand 31 remain low. As a consequence of the

output signal r180 going high, the "update outer" signal goes high, with the "update inner" signal remaining low, indicating that a phase error of magnitude >T/4 has occurred.

The method and strategy described above can readily be adapted to provide a method for estimating any asymmetry/skew error between the clock and data pulses. In a system with no skew error, the data pulse position should jitter around the centre of the clock window with zero mean. In a practical system, however, various noise imperfections can result in the mean jitter being non-zero. This will degrade the data synchroniser window margin and hence overall system performance. It is desirable, therefore, to be able to identify any skew present to enable correction by some additional circuitry. A measurement of the skew present in the system can be achieved by a simple re-arrangement of the circuit of FIG. 6 so that one of the counters accumulates negative phase errors and the other positive phase errors. This circuit re-arrangement is shown in FIG. 8.

In this second embodiment, the apparatus 12 is used to calculate skew error, or asymmetry in the data window, but otherwise all the elements that were described with reference to FIG. 6 are the same, and have been given the same reference numbers, except that the outputs of the registers in the second set have been rearranged so that the outputs of registers 31 and 34, corresponding to the phase windows clocked by clocks clk0 and clk270, are coupled to OR gate 35 to provide an "update positive" signal and the outputs of registers 32 and 33, corresponding to the phase windows clocked by clocks clk90 and clk180, are coupled to OR gate 36 to provide an "update negative" signal. Again, when no data edge pulses are present then no update signals are provided to the counters.

For this embodiment, a minor modification is also required to the comparator 14 of FIG. 5, so that the result of the second (M-bit) counter 13 is latched when the first (N-bit) counter 12 reaches, for example, 2^{M-1}. Any asymmetry will be reflected by the amount of deviation of the latched value relative to 2^{M-1}. Clearly if the window is symmetric there should be an equal number of positive and negative phase errors. If the latched value is greater, then the asymmetry is positive and if the latched value is smaller, then the asymmetry is negative. This information can be supplied to additional

circuitry which can be used to compensate for the asymmetry effects and re-centre the clock window.

It will be appreciated that although only two particular embodiments of the invention have been described in detail, various modifications and improvements can be made by a person skilled in the art without departing from the scope of the present invention.

CLAIMS

1. A method of estimating an error in a data recovery system, the method comprising the steps of:

receiving data pulses at a data rate;

receiving a plurality of clock signals, the clock signals having the same rate as the data rate but being substantially equally phase offset from one another;

clocking the data pulses with each of the clock signals to determine at which phase offset each data pulse is received;

counting the number of data pulses received at different phase offsets to provide a value representing a statistical ratio of the counts at different clock phase offsets; and

utilizing the value representing the statistical ratio to determine an error for the received data pulses.

2. A method of estimating an error according to claim 1, wherein the step of clocking the data pulse comprises:

applying the data pulses to each of a plurality of registers, each clocked by a different one of the plurality of clock signals; and

determining which of the plurality of registers first clocks each data pulse.

3. A method of estimating an error according to claim 2, wherein the step of counting the number of data pulses received at different phase offsets comprises:

incrementing one of a plurality of counters each time a register associated with that counter is determined to have first clocked a particular data pulse; and

determining the count of at least one counter when at least one other counter reaches a predetermined value.

4. A method of estimating an error according to claim 1, wherein the step of utilizing the value representing the statistical ratio to determine an error comprises:

checking a look-up table for an error rate corresponding to the value.

5. A method of estimating an error according to any preceding claim, wherein there are four clock signals which are in a quadrature phase relation.

6. A method of estimating an error according to claim 5, wherein the step of counting the number of data pulses received at different phase offsets comprises:

incrementing a first counter when either one of two registers clocked by clock signals having phase offsets of 0° and 90° first clocks a particular data pulse or incrementing a second counter when either one of two registers clocked by clock signals having phase offsets of 180° and 270° first clocks a particular data pulse;

determining when one of the two counters reaches a predetermined value; and

determining the count of the other of the two counters; and wherein the count of the other counter is then used to determine an error rate from a look-up table.

7. A method of estimating an error according to claim 5, wherein the step of counting the number of data pulses received at different phase offsets comprises:

incrementing a first counter when either one of two registers clocked by clock signals having phase offsets of 0° and 270° first clocks a particular data pulse or incrementing a second counter when either one of two registers clocked by clock signals having phase offsets of 90° and 180° first clocks a particular data pulse;

determining when one of the two counters reaches a predetermined value; and

determining the count of the other of the two counters; and wherein the count of the other counter is then compared to the predetermined value and used to determine whether a skew error is positive or negative.

8. Apparatus for estimating an error in a data recovery system, the apparatus comprising:

a data terminal for receiving data pulses at a data rate;

a plurality of clock input terminals for receiving a plurality of clock signals, the clock signals having the same rate as the data rate but being substantially equally phase offset from one another;

data clocking device having a data input coupled to the data terminal, a plurality of clock inputs coupled to the plurality of clock input terminals and a plurality of outputs, each providing a count signal when a data pulse is clocked by a clock signal at an associated clock input;

a plurality of counters, each having a count input coupled to at least one of the plurality of outputs of the data clocking means for counting the number of data pulses received at different phase offsets to provide a value representing a statistical ratio of the counts at different clock phase offsets; and

a device having an input coupled to the output of at least one of the plurality of counters and an output to provide an error for the received data pulses based on the counts at different clock phase offsets.

9. Apparatus for estimating an error in a data recovery system according to claim 8, wherein the data clocking means comprises:

a plurality of registers, each register having a first input coupled to the data input, a second input and an output, each of the second inputs of the plurality of registers being coupled to a different one of the plurality of clock inputs; and

a discriminating device having a plurality of inputs coupled to the outputs of the plurality of registers and a second plurality of outputs, wherein only one of the outputs provides a count signal for each data pulse received depending on which register was the first to clock the particular data pulse.

10. Apparatus for estimating an error in a data recovery system according to claim 9, wherein at least one counter has a maximum value associated therewith and provides an indication at an output thereof when that maximum value has been reached, and at least one other counter provides at an output thereof an indication of the value it has reached when the at least one counter has reached the maximum value.

11. Apparatus for estimating an error in a data recovery system according to any one of claims 8, 9 or 10, wherein there are four clock signals which are in a quadrature phase relation.

12. Apparatus for estimating an error in a data recovery system according to claim 11, wherein there are four registers, each receiving one of the four clock signals at the second input thereof.

13. Apparatus for estimating an error in a data recovery system according to claim 12, wherein the discriminating device comprises:

a four input NOR gate, the four inputs being coupled to the four outputs of the four registers, and an output;

four multiplexers, each having a first input coupled to a respective output of a respective one of the four registers, a second input coupled to an output of the multiplexer, and a control input coupled to the output of the NOR gate;

four second registers, each of the second registers having a first input coupled to a respective output of a respective multiplexer, a clock input coupled to receive a system clock signal, and an output; and

a first OR gate having first and second inputs coupled to the outputs of two of the second registers and an output, and a second OR gate having first and second inputs coupled to the outputs of the other two of the second registers and an output.

14. Apparatus for estimating an error in a data recovery system according to claim 13, wherein the first OR gate has its first and second inputs coupled to the outputs of the two second registers corresponding to the two registers

clocked by clock signals having phase offsets of 0° and 90° and the second OR gate has its first and second inputs coupled to the outputs of the two second registers corresponding to the two registers clocked by clock signals having phase offsets of 180° and 270°.

15. Apparatus for estimating an error in a data recovery system according to claim 14, wherein a first counter is incremented when either one of two registers clocked by clock signals having phase offsets of 0° and 90° first clocks a particular data pulse and a second counter is incremented when either one of two registers clocked by clock signals having phase offsets of 180° and 270° first clocks a particular data pulse.

16. Apparatus for estimating an error in a data recovery system according to claim 15, wherein the device includes a look-up table which provides an error rate for the received data pulses based on the ratio of the values of the two counters.

17. Apparatus for estimating an error in a data recovery system according to claim 13, wherein the first OR gate has its first and second inputs coupled to the outputs of the two second registers corresponding to the two registers clocked by clock signals having phase offsets of 0° and 270° and the second OR gate has its first and second inputs coupled to the outputs of the two second registers corresponding to the two registers clocked by clock signals having phase offsets of 90° and 180°.

18. Apparatus for estimating an error in a data recovery system according to claim 17, wherein a first counter is incremented when either one of two registers clocked by clock signals having phase offsets of 0° and 270° first clocks a particular data pulse and a second counter is incremented when either one of two registers clocked by clock signals having phase offsets of 90° and 180° first clocks a particular data pulse.

19. Apparatus for estimating an error in a data recovery system according to claim 18, wherein the device includes a comparator to determine which of the two counters has a higher value so as to provide an indication of whether a skew error is positive or negative.

20. Apparatus for estimating an error in a data recovery system substantially as hereinbefore described with reference to FIGS. 5 to 7 or FIG. 8 of the accompanying drawings.

21. A method of estimating an error in a data recovery system substantially as hereinbefore described with reference to FIGS. 5 to 7 or FIG. 8 of the accompanying drawings.

22. A data recovery system incorporating apparatus for estimating an error according to any one of claims 8 to 20.

A METHOD AND APPARATUS FOR ESTIMATION OF ERROR IN DATA RECOVERY SCHEMES

ABSTRACT

An on-chip data independent method and apparatus for channel error estimation in a data recovery scheme is based on measuring phase noise statistics. The apparatus (10) receives a data pulse and four quadrature clock signals and has a discriminating device (11) to provide a count signal for each data pulse received depending on which clock signal was the first to clock the particular data pulse. A pair of counters (12 and 13) counts the number of data pulses received at different phase offsets to provide a value representing a statistical ratio of the counts at different clock phase offsets from which an error rate for the received data pulses based on the counts at different clock phase offsets can be determined from a look-up table (16). By re-configuring the circuitry, the system can be adapted to measure clock window asymmetry.

FIG. 5

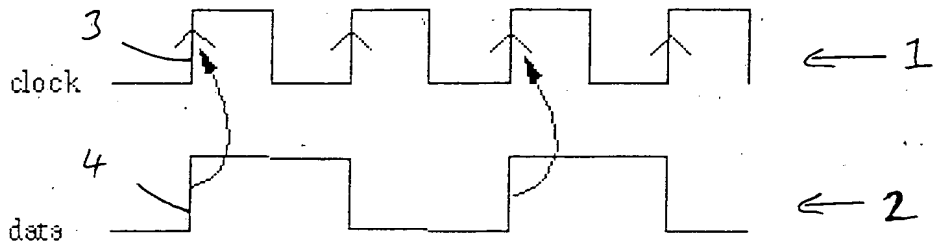

FIG. 1

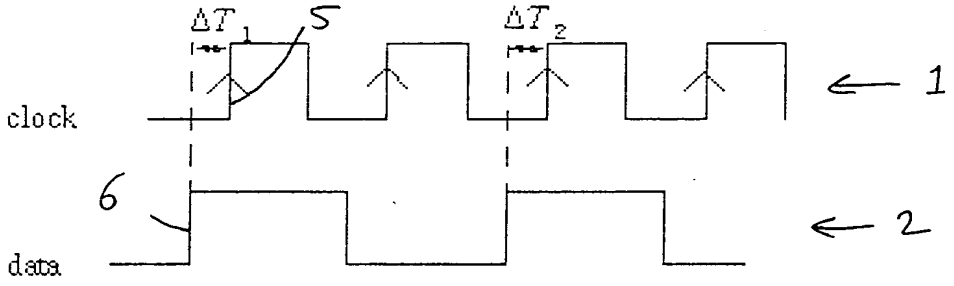

FIG. 2

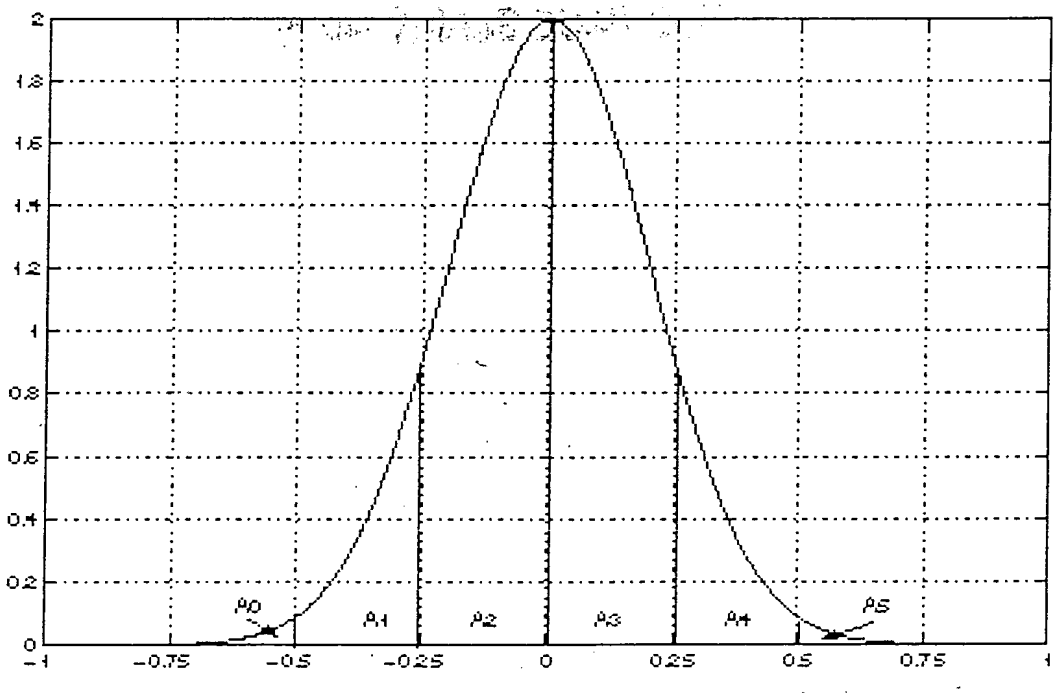

FIG. 3

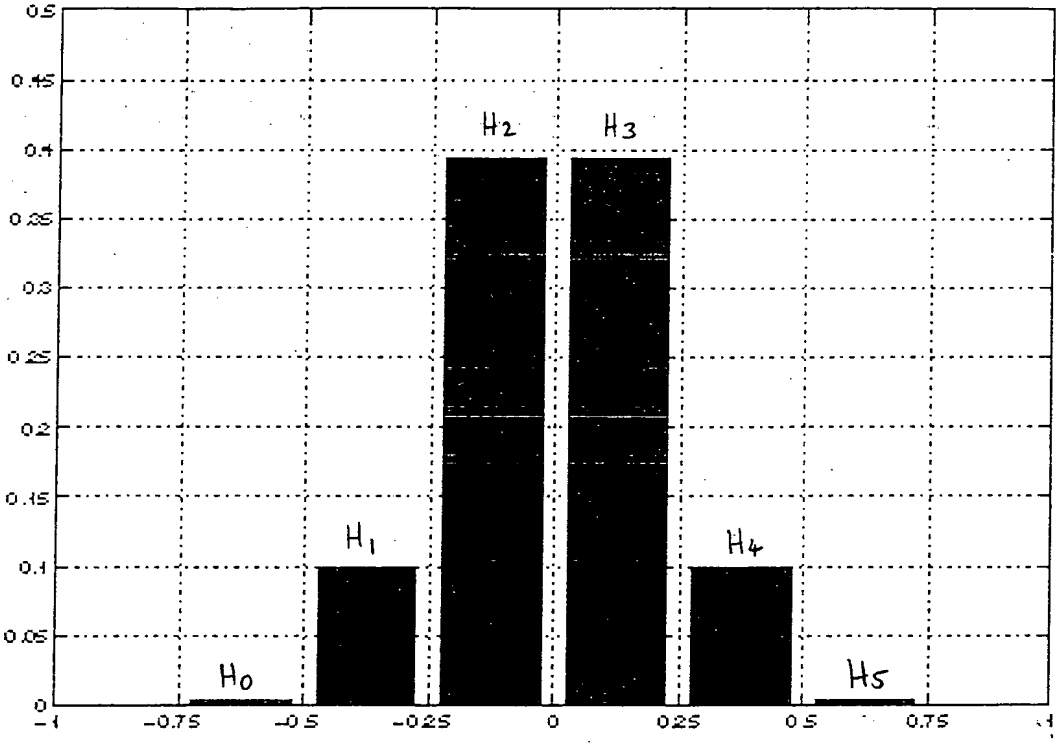

FIG. 4

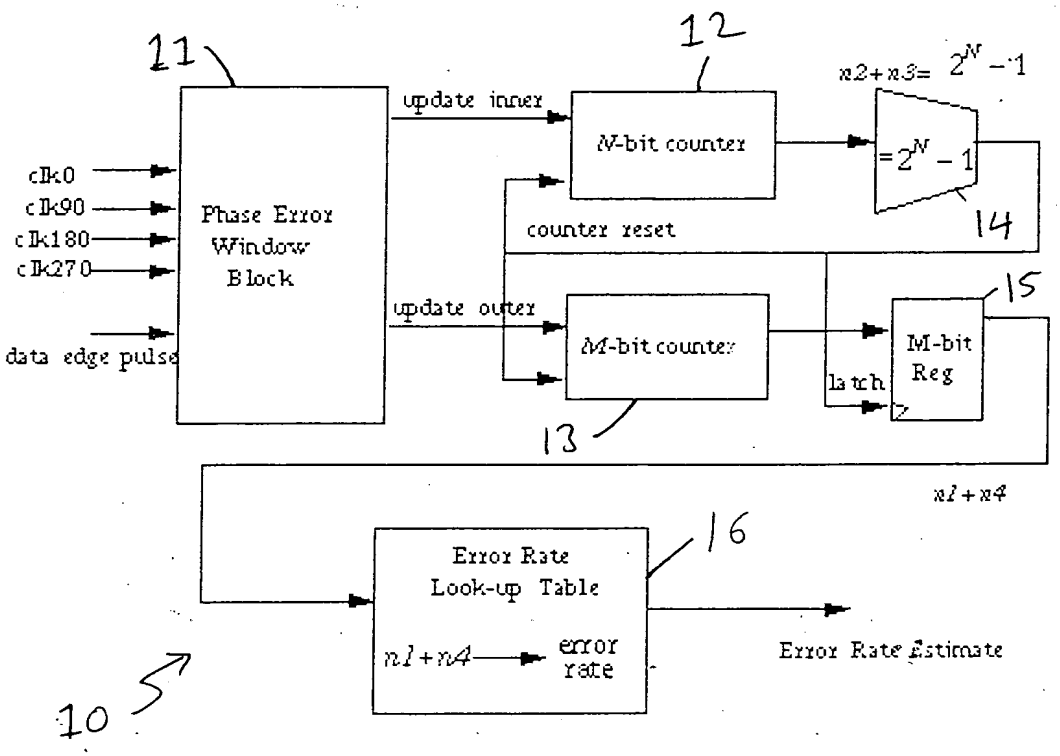

FIG. 5

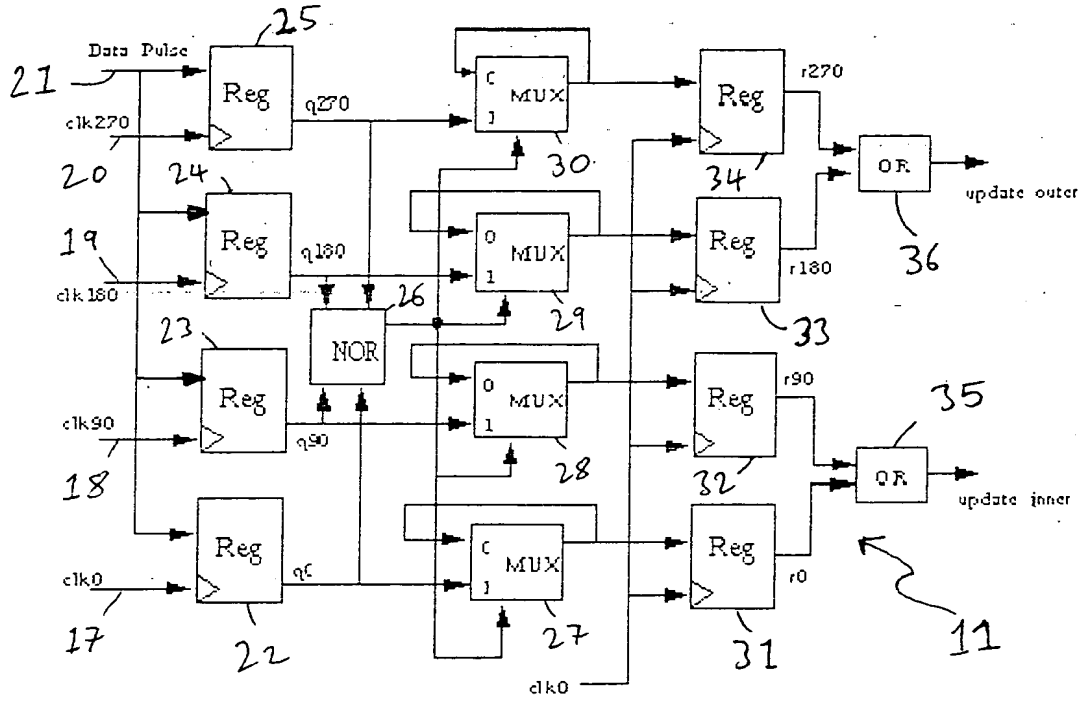
Data Pulse
21
clk270
20
clk180
19
clk90
18
clk0
17
Reg
25
24
23
22
q270
q180
q90
q0
NOR
26
MUX
30
29
28
27
r270
r180
r90
r0
34
33
32
31
OR
36
35
update outer
update inner
11
clk0

FIG. 6

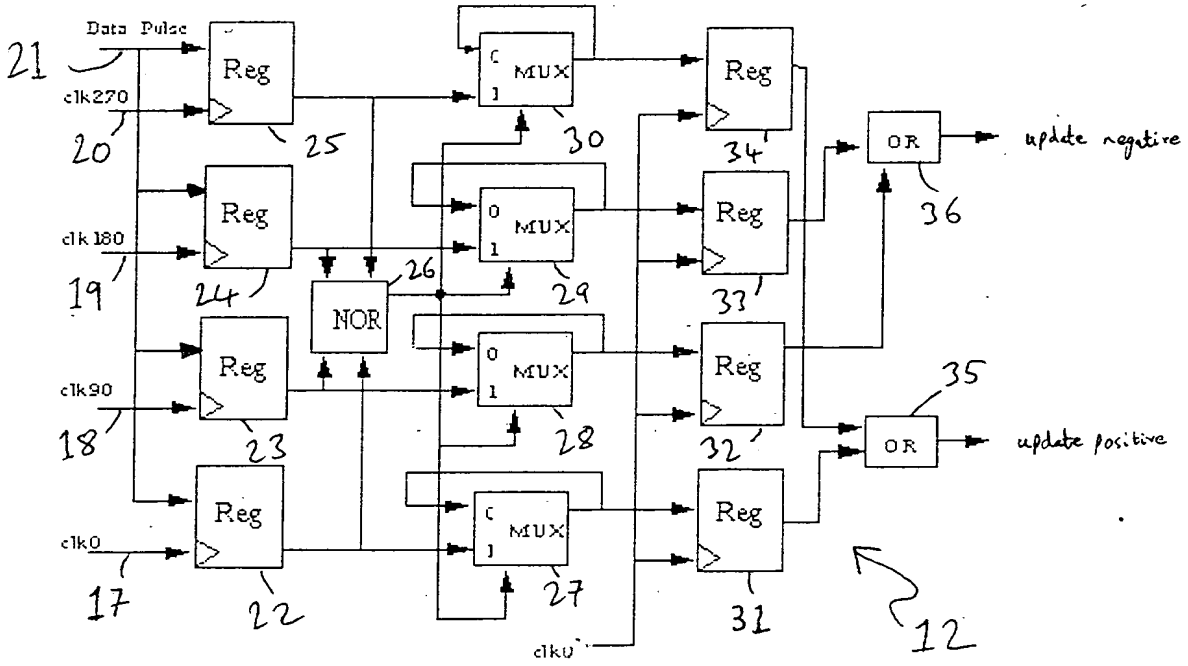
Data Pulse
21
clk270
20
clk180
19
clk90
18
clk0
17
Reg
25
24
23
22
NOR
26
MUX
30
29
28
27
34
33
32
31
OR
36
35
update negative
update positive
12
clk0

FIG. 8

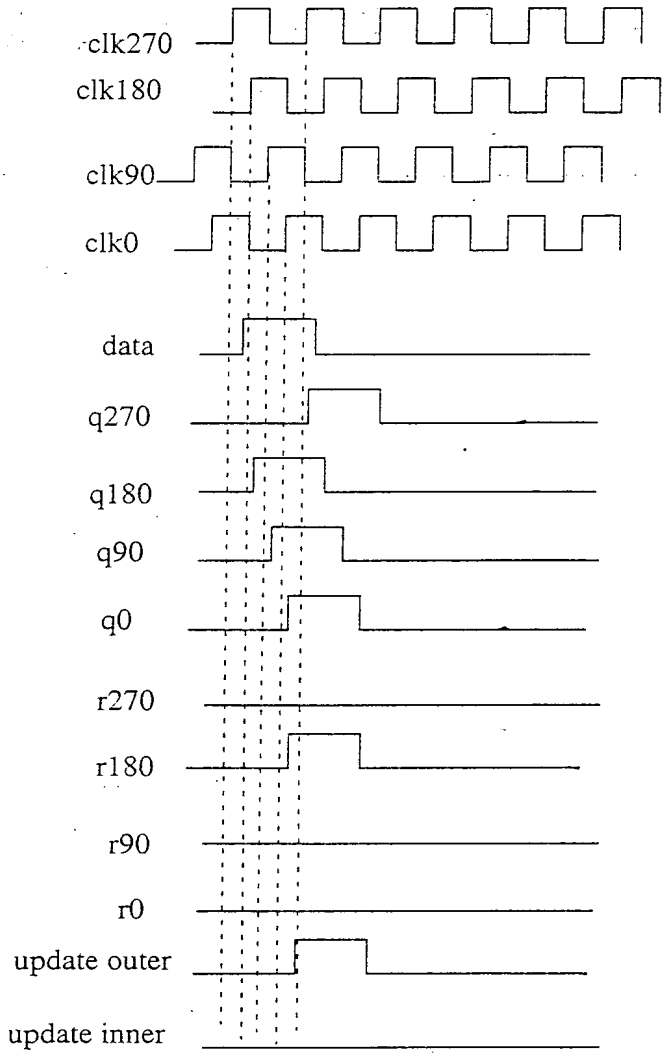
clk270
clk180
clk90
clk0
data
q270
q180
q90
q0
r270
r180
r90
r0
update outer
update inner

FIG. 7